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Design of Silicon Carbide and Gallium Nitride Power Devices for Electric Vehicle Applications

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Abstract:
In a battery electric vehicle, every watt of power wasted by the power converters is a watt lost from range, charging speed and cooling headroom. Silicon carbide (SiC) and gallium nitride (GaN) power devices reduce those losses and allow higher switching frequencies than silicon, but they do so with different device physics and different packaging problems. The study is comparative and analytical, and no new experiments were conducted. We compare vertical 4H-SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) with lateral enhancement-mode AlGaN/GaN high-electron-mobility transistors (HEMTs). We correlate drift-region and two-dimensional-electron-gas design to blocking voltage and on-state resistance. Then, a loss and junction-temperature framework is applied to two manufacturer datasheets, a 1200V SiC MOSFET and a 600V GaN HEMT, with different ratings and test conditions are provided with explicitly specified. A first-order analytical model puts the frequency at which switching loss overtakes conduction loss near 43 kHz for the SiC example and near 74 kHz for the GaN example, whose switching energy is estimated rather than measured. A sourced timeline shows how each technology reached vehicle-relevant ratings. Published work on traction inverters, onboard chargers, DC–DC converters, and auxiliary stages points to SiC for high-current inverters and 800V systems, and to GaN for compact, high-frequency stages at 650V and below. The major trade-offs are gate-oxide stability, short-circuit capability, dynamic on-resistance, package inductance and automotive qualification. We enumerated the research gaps they create.
Keywords:
electric vehicles, gallium nitride, high-frequency converters, power electronics, power MOSFETs, wide-bandgap semiconductors, silicon carbide..

1. INTRODUCTION

Every watt of waste from the vehicle's power electronics comes out of the battery, and then the coolant loop has to carry it away. The traction inverter, the onboard charger (OBC) and the DC–DC converters are all part of the main energy path, and their efficiency, size and temperature limits directly influence the range, charging time and packaging. Chargers feel this most, since weight, space, and cost on board the vehicle are tightly capped [1].

Silicon insulated-gate bipolar transistors (IGBTs) and super junction MOSFETs still carry most of this load. Due to the tail current, the reverse-recovery charge and the output capacitance they do not switch fast without losing efficiency. Wide-bandgap (WBG) semiconductors break down at a critical electric field several times higher than silicon's, so a drift region of a given blocking voltage can be thinner and more heavily doped [2], [3]. Currently, there are two families of WBG, SiC, mainly vertical power

MOSFETs, and GaN, mainly lateral enhancement mode high-electron-mobility transistors (HEMTs) rated at 650 V and below [2], [4].

Which one it is depends on where it is located in the powertrain. SiC devices have been used in traction inverters and high voltage DC–DC converters [3], [5]. GaN was shown to operate at high frequency on-board chargers [6]. The choice between them is simply a matter of selecting a device that will meet the voltage, current, frequency and thermal conditions of one stage, and its rating and package. That is not decided by the material properties alone. The answer is shifted by gate drive, parasitic inductance, the cooling path and long-term reliability.

This paper is a design study based on the published literature and two manufacturer datasheets [4], [7]. No experiments or circuit simulations were performed. It correlates device structure to the parameters a designer will use, develops a single loss and junction-temperature framework, follows the path of each technology to vehicle-relevant ratings, and assesses suitability for traction inverters, onboard chargers, DC-DC converters, auxiliary converters, and 800 V architectures. Throughout, when using values from the datasheet, values we derived from the datasheet, or first order estimates, this is indicated, and any rating mismatches between the two example devices are called out. Section 2 and Section 3 deal with the history, the materials and the structures of the devices. Section 4 develops the loss framework, Section 5 looks at the EV subsystems, and Sections 6 and 7 compare the technologies and discuss thermal and reliability issues. Sections 8 and 9 are devoted to open problems and conclusions.

2. FUNDAMENTALS OF SIC AND GAN POWER DEVICES

A. Material properties & figures of merit

Table 1 Typical room temperature properties of Silicon, 4H-SiC and GaN [8], [9]. The bandgap determines the intrinsic carrier concentration and the critical field E_c for the onset of avalanche breakdown by impact ionization. For an ideal one-dimensional unipolar drift region the specific on resistance cannot be smaller than [8]

Table 1: Room-temperature material properties [8], [9]

Property	Si	4H-SiC	GaN
Bandgap (eV)	1.12	≈3.2	≈3.4
Critical field E_c (MV/cm)	≈0.3	≈2–3	≈3–3.5
Electron mobility, bulk ($cm^2/V·s$)	≈1400	≈800–1000	≈1000–1200
Electron mobility, 2DEG ($cm^2/V·s$)	n/a	n/a	≈1500–2000
Thermal conductivity (W/cm·K)	≈1.5	≈3.7–4.9	≈1.3–2.0
Relative permittivity	≈11.7	≈9.7	≈9
Typical power-device structure	Vertical	Vertical	Lateral (on Si)

$$R_{\mathrm{on,sp}} \geq \frac{4{V_{\mathrm{BR}}}^2}{\varepsilon_s \mu_n {E_c}^3} \quad (1)$$

where V_{BR} is the breakdown voltage, ε_s the permittivity, and μ_n the electron mobility of the drift region. Because E_c enters cubed, a critical field roughly eight times silicon's cuts the ideal limit in (1) by orders of magnitude at the same voltage. Real devices are miles away from it. The total is made up of channel, JFET (junction field-effect transistor), contact, and substrate resistance, and the gap between ceiling and product is quite different for SiC and GaN.

Bulk mobility is just part of the story. Scattering at the SiC/SiO_2_interface degrades the channel mobility in SiC MOSFETs well below the bulk value [9]. In GaN HEMTs, the two-dimensional electron gas (2DEG) at the AlGaN/GaN interface is characterized by high sheet charge and high mobility without intentional doping but its stability under high field relies on the charge trapped in the buffer and at the surface [10]. Heat conduction is favorable to SiC with its good substrate for heat

movement. GaN power devices are typically grown on foreign substrates such as silicon, and so the heat has to go through the buffer and substrate. It is not the conductivity of GaN that is limiting the thermal path.

Switching behavior is more dependent on charges and capacitances than material constants: gate charge Q_G, output capacitance Coss with stored energy E_{oss}, and reverse-recovery charge. Values are set by device geometry, epitaxy and package and a material figure of merit showing potential and little else. The performance of the device is defined by the substrate and epitaxial quality, cell design, gate drive, circuit parasitics and cooling. Therefore Sections 4 to 7 compare complete devices and converters.

B. Historical development and relevance to EVs

In Fig. 1 we show the milestones we found and what they meant to vehicles. The order matters because you can only use a device concept in a car once you have ratings, qualification evidence and a matching package. The gate injection transistor of 2007 solved the normally-off problem that kept the two-dimensional electron gas outside of switching converters [11] on the GaN side. In 2010 Efficient Power Conversion announced what it called the first enhancement-mode GaN-on-silicon power transistors for power management, not traction [12]. In January 2011, Cree announced the first fully qualified commercial SiC power MOSFET with a voltage rating of 1200V and 80 mΩ [13]. Both "first" claims are from the manufacturers themselves, and we did not independently verify them.

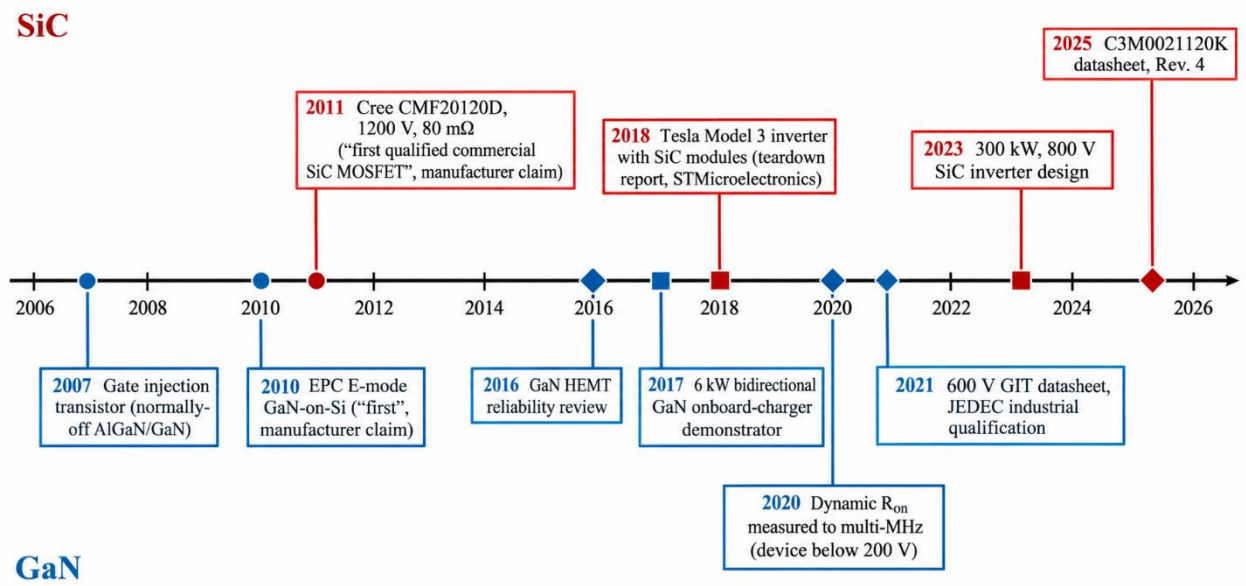

Fig. 1. Milestones in SiC and GaN Power Devices for EVs Circles are used to launch devices or products. Squares are for vehicle level applications or demos. Diamonds are for reliability evidences or datasheets used in this paper. Those marked "claim" are statements from the manufacturer. Sources: [4], [5], [6], [7], [10], [11], [12], [13], [14], [15].

Then came the vehicle adoption. In 2018, a market-research teardown found a full SiC power module in the Tesla Model 3 inverter, developed with STMicroelectronics [14]. The work published in 2023 was discussing 300 kW, 800 V SiC inverters [5]. In 2017, GaN was used to build a 6-kW bidirectional on-board charger demonstrator for vehicle charging [6]. However, the reliability studies carried out in 2016 and 2020 identified trapping and dynamic on-resistance as the main challenges [10], [15]. The two analyzed datasheets are from the latest stage: a 600 V GaN device with industrial qualification based on JEDEC from 2021 [4] and a 1200 V SiC MOSFET from 2025 [7].

Looking at the timeline in sequence, SiC seems to have first achieved automotive-class voltage and current, which is appropriate for traction inverters. GaN moves in bunches, at 650 V and below, where high frequency makes sense. This is not what the sources are saying. It was our own interpretation of the sequence, and a milestone not verified here was absent from the chart.

3. DEVICE STRUCTURES AND DESIGN METHODOLOGY

A. Vertical 4H-SiC MOSFETs

Commercial power devices [9] use the 4H polytype. The planar vertical cell is shown in Fig. 2(a). It comprises an n^+ substrate, an n^- epitaxial drift layer for the blocking voltage, p-wells with n^+ source and p^+ body contacts, a gate oxide and a polysilicon gate. Current flows laterally through the channel in the p-well, squeezes through the JFET region between the wells, and runs vertically down the drift layer to the drain.

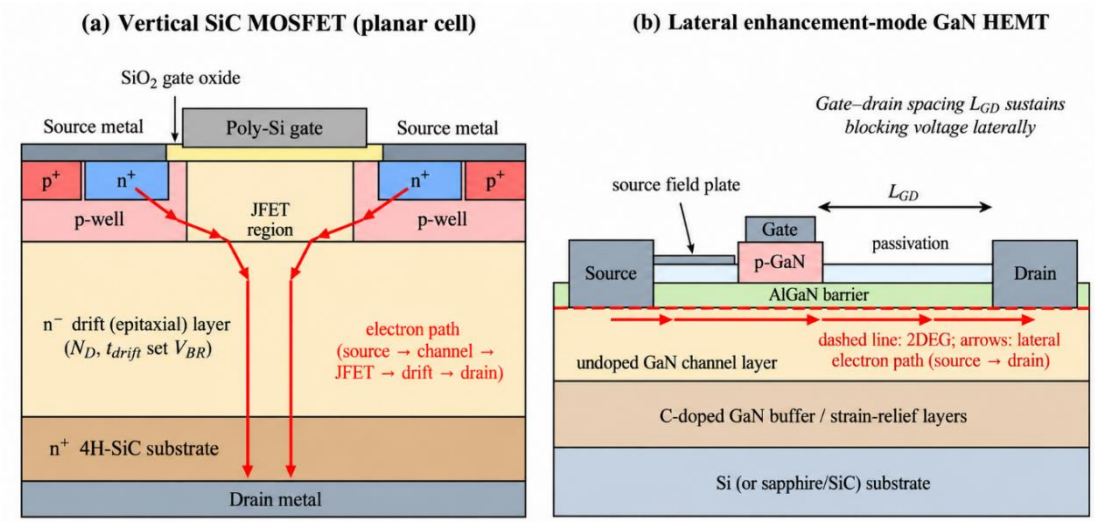

Fig. 2. Simplified cross-sections (not to scale). (a) Vertical planar SiC MOSFET cell. (b) Lateral p-GaN-gate enhancement-mode GaN HEMT with source-connected field plate. Red arrows show the current path of electrons. The author's original scheme, inspired by the structures described in [9], [11].

For an abrupt 1-D junction without punchthrough the drift-layer thickness and doping are set by the critical field [8]:

$$W_{\mathrm{D}} = \frac{2V_{\mathrm{BR}}}{E_{\mathrm{c}}} \tag{2}$$

$$N_{\mathrm{D}} = \frac{\varepsilon_{\mathrm{s}} {E_{\mathrm{c}}}^2}{2qV_{\mathrm{BR}}} \tag{3}$$

with q the elementary charge. Assuming E_c = 2.5 MV/cm and $\varepsilon_s = 9.7\ \varepsilon_0$, (2) and (3) give a 1200 V device about 9.6 µm of drift layer doped to roughly 1.4×10^{16} cm^{-3}. With μ_n = 950 cm^2/V·s, (1) then gives an ideal specific on-resistance of about 0.45 mΩ·cm^2. All three results are calculated ideals. In practice the doped layers are thicker or lighter for margin, and the channel and JFET regions add resistance not accounted for in the ideal formula.

The design is driven by three specific issues of SiC. The oxide interface limits channel mobility, so the designers shrink the cells to increase the channel density and drive the gate at a high positive voltage. The 1200 V datasheet example specifies a turn-on of 15 V and a static off-state drive of −4 V, with a transient absolute range of −8 V to +19 V [7], a smaller margin than that of silicon MOSFETs. Gate-bias stress has been used to attribute the threshold voltage shift to near-interfacial oxide traps [16]. And the intrinsic body diode has a large forward drop (4.6 V typical at -4 V gate bias and 25 A in the same datasheet [7]), while its bipolar conduction can degrade the crystal through basal-plane defects [9]. To counter this, designers reduce dead time, add an external diode or turn the channel on synchronously during reverse conduction.

B. Lateral enhancement-mode GaN HEMTs

The lateral structure is shown in Fig.2(b). The polarization in the AlGaN/GaN heterostructure causes a 2DEG without any doping . This is why a regular HEMT is normally on . The p-GaN gate, introduced as the gate injection transistor for power switching, depletes the 2DEG at zero bias. At positive gate bias hole injection increases the channel electron density via conductivity modulation and the original device was reported to have a threshold on the order of +1 V [11].

Because the channel is the 2DEG, on-resistance follows from the sheet resistance in (4) and the device geometry in (5), not from a drift-layer formula:

$$R_{\mathrm{sh}} = \frac{1}{q n_{\mathrm{s}} \mu_{\mathrm{2DEG}}} \tag{4}$$

$$R_{\mathrm{DS(on)}} \approx R_{\mathrm{c}} + R_{\mathrm{sh}} \cdot \frac{L_{\mathrm{SG}} + L_{\mathrm{G}} + L_{\mathrm{GD}}}{W} \tag{5}$$

where n_s is the 2DEG sheet density, μ_{2DEG} its mobility, R_c the total contact resistance, L_{SG}, L_G, and L_{GD} the source–gate, gate, and gate–drain lengths, and W the gate width. The voltage is blocked laterally across L_{GD}, so higher ratings need longer access regions and more chip area. In the vertical SiC device, thickness scales with voltage instead. Field plates, shown in Fig. 2(b), flatten the peak field at the gate edge, and the carbon-doped buffer limits leakage and supports the voltage vertically [10].

The datasheet example is current driven. On-resistance is specified at a gate current of 26.1 mA, the continuous average gate current is limited to 20 mA, and the threshold is 1.2 V typical at 25 °C, falling to 1.0 V at 125 °C [4]. A gate driver for this part needs more specialized design than a SiC driver does. In reverse conduction there is no body diode and no reverse-recovery charge, only output charge, yet the third-quadrant drop is 2.2 V typical at 8 A with the gate at 0 V [4], so dead time still costs efficiency. Trapping causes dynamic on-resistance, a rise in resistance right after off-state stress [10]. One measurement on a commercial sub-200 V HEMT found an increase of at most 2× the DC value in a multi-megahertz zero-voltage-switched application [15]. Extrapolating to 650 V devices needs voltage-specific data.

C. Vertical design vs. lateral design

The two structures fail and cool in different ways. In the vertical SiC device, the heat flows from the active surface through the drift layer and conductive substrate to a drain metal on the bottom side. A large cell array shares the current, which is good for power modules. In the lateral GaN device the current is flowing in a thin layer near the surface, the active volume is small, and the heat dissipation depends on the buffer, the substrate and the orientation of the package. The GaN products commercialized here are lateral products. We distinguish between commercial, qualified structures and research-stage ones, and the quantitative statements below only pertain to the former.

4. ELECTRICAL AND SWITCHING PERFORMANCE ANALYSIS

To make a fair comparison, all devices need to be specified with the same parameters: rated blocking voltage, on-resistance as a function of temperature, switching energy at specified conditions, gate-drive voltage and charge, limit for junction temperature, thermal resistance and package parasitics. They are gathered in Table 2 from the two datasheets [4], [7]. The devices are in different voltage classes (1200 V, 600 V) and were tested at different bus voltages and currents, therefore the table summarizes data and does not rank anything.

Table 2: Parameters of datasheet of two representative commercial devices [4], [7]. The devices differ in voltage class and test conditions and are not directly equivalent. Typical values unless otherwise noted.

Parameter	SiC MOSFET, C3M0021120K [7]	GaN HEMT, IGOT60R070D1 [4]
Structure; package	Vertical planar SiC MOSFET; TO-247-4 with driver-source pin	Lateral p-GaN-gate HEMT; PG-DSO-20-87
Rated V_{DS}	1200 V	600 V (750 V pulsed)
Continuous I_D	100 A at T_C = 25 °C; 74 A at 100 °C	31 A at T_C = 25 °C
$R_{DS(on)}$ at 25 °C	21 mΩ (max 28.8 mΩ), 15 V, 50 A	55 mΩ (max 70 mΩ), I_G = 26.1 mA, 8 A
$R_{DS(on)}$ at high T_j	38 mΩ at 175 °C	100 mΩ at 150 °C
Gate drive	−4 V / +15 V, voltage driven	Current driven; $I_{G,avg} \leq$ 20 mA; $V_{GS} \geq -10$ V
Gate charge Q_G	162 nC (800 V, 50 A)	5.8 nC (400 V, 8 A)
$R_{DS(on)} \cdot Q_G$ at 25 °C	3402 mΩ·nC	319 mΩ·nC
C_{oss}; E_{oss}	180 pF at 1000 V; 99 µJ	72 pF at 400 V; Q_{oss} = 41 nC

Parameter	SiC MOSFET, C3M0021120K [7]	GaN HEMT, IGOT60R070D1 [4]
$E_{on} + E_{off}$	0.69 + 0.42 mJ (800 V, 50 A, 175 °C, $R_{G(ext)}$ = 2.5 Ω, SiC diode)	Not specified
Switching times ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f)	29, 33, 57, 14 ns (800 V, 50 A)	10, 8, 14, 15 ns (400 V, 8 A)
Reverse conduction	Body diode, V_{SD} = 4.6 V at 25 A, −4 V; Q_{rr} = 928 nC	V_{SD} = 2.2 V at 8 A, 0 V; Q_{rr} = 0 (excl. Q_{oss})
$R_{\theta JC}$; max T_j	0.32 °C/W; 175 °C	≤ 1 °C/W; 150 °C
Qualification statement	None stated in the datasheet extract	JEDEC JESD47/JESD22, industrial

For a switch carrying rms current I_{rms}, conduction loss is [8]

$$P_{cond} = {I_{rms}}^2 R_{DS(on)}(T_j) \quad (6)$$

The product form in (6) assumes a resistive on state with the same I_{rms} flowing for the full conduction interval. I_{rms} to operate in and whether a threshold or knee voltage needs to be added is a function of the waveform, duty cycle and conduction mode. The resistance increases with junction temperature and (7) approximates it linearly:

$$R_{DS(on)}(T_j) \approx R_{DS(on),25}\left[1 + \alpha_R(T_j - 25)\right] \quad (7)$$

where α_R is an average temperature coefficient. The datasheet values in Table 2 give $\alpha_R \approx 0.0054\ K^{-1}$ for the SiC device (25 to 175 °C) and $\approx 0.0065\ K^{-1}$ for the GaN device (25 to 150 °C, at 8 A). Both were averages, and they neglect dependence on current or gate voltage. The switching loss is approximated as

$$P_{sw} = f_{sw}(E_{on} + E_{off}) \quad (8)$$

with f_{sw} the switching frequency and E_{on}, E_{off} the energies per transition. The energies in (8) depend on bus voltage, current, gate resistance, junction temperature, layout inductance, and the commutating device. The SiC datasheet shows the last dependence clearly: replacing the SiC freewheeling diode with the MOSFET body diode raises the sum $E_{on} + E_{off}$ from 1.11 mJ to 1.92 mJ [7]. Gate-drive power follows $P_G = Q_G \Delta V_G f_{sw}$. At 100 kHz and a 19V gate swing which is about 0.31W per SiC device, small compared to the other terms.

Switching energies are not provided in the GaN datasheet, so we estimated them from its inductive switching times and capacitances. A linear voltage–current overlap model plus the stored energy in the output capacitance gives

$$E_{ov} \approx \frac{1}{2} V_{DC} I_L (t_r + t_f) \quad (9)$$

$$E_{oss} = \frac{1}{2} C_{o(er)} {V_{DC}}^2 \quad (10)$$

with V_{DC} the bus voltage, I_L the load current, t_r and t_f the datasheet rise and fall times, and $C_{o(er)}$ the energy-related effective output capacitance, 80 pF between 0 and 400 V [4]. At 400 V and 8 A, (9) gives 36.8 µJ and (10) gives 6.4 µJ, an estimated 43 µJ per cycle. The estimate is first order, and assumes hard switching. It also relies on datasheet times measured at a gate drive which may not be representative of a real design and ignores the stored energy and dynamic on-resistance of the complementary device.

Setting switching loss equal to conduction loss defines a corner frequency,

$$f^* = \frac{P_{cond}}{E_{on} + E_{off}} \quad (11)$$

Evaluating (6), (8), and (11) at the datasheet test points and a duty cycle of 0.5, the SiC example (800 V, 50 A, 175 °C) has P_{cond} = 47.5 W, 111 W of switching loss at 100 kHz, and $f^* \approx 43$ kHz. The GaN example (400 V, 8 A, resistance at 150 °C) has P_{cond} = 3.2 W, an estimated 4.3 W of switching loss at 100 kHz, and $f^* \approx 74$ kHz. Fig. 3 plots both totals normalized by $V_{DC} I_L D$. Normalizing removes the difference in power level but not the difference in voltage class.

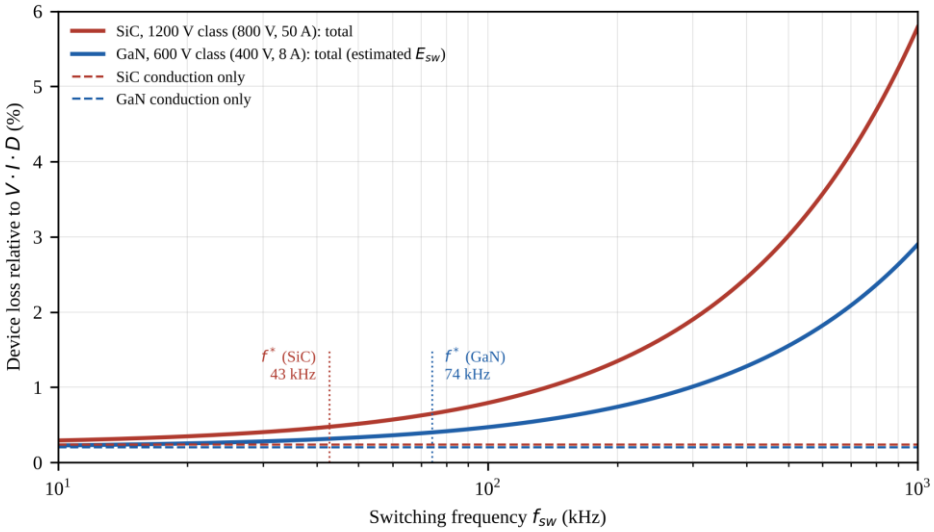

Fig. 3. Illustrative analytical model of per-switch loss (conduction plus switching) relative to $V_{DC}I_LD$ versus switching frequency, for hard switching at duty cycle 0.5. SiC: 800 V, 50 A, $R_{DS(on)}$ = 38 mΩ, E_{on} + E_{off} = 1.11 mJ, from [7]. GaN: 400 V, 8 A, $R_{DS(on)}$ = 100 mΩ from [4], with switching energy of 43 µJ estimated from (9) and (10). Modelled values, not measurements. The two devices are in different voltage classes.

Fig. 3 shows the shape of the two curves and should not be read as a ranking. Switching loss dominates both totals at high frequency. The GaN curve is lower mainly because of its lower voltage class and because its switching energy is an estimate. Soft switching eliminates much of the overlap and stored-energy loss, and would shift both curves, favoring the device with the lower output charge. Device loss is a single term only at converter level. Magnetics, capacitors, cooling and EMI filters all change with frequency, so they all have to be included in the optimization. The losses of IGBT and SiC inverters have been compared for 400 V and 800 V DC bus [17]. Such results are applicable to the bus voltage and drivetrain studied.

5. APPLICATION-SPECIFIC DESIGN FOR ELECTRIC VEHICLES

The technologies are located in the powertrain in Fig. 4 and their suitability is summarized in Table 3. The table is our own engineering synthesis of the literature and datasheets listed. It is a reflection of the design drivers for each phase and not a measured ranking

A. Traction inverters

An inverter combines maximum power and maximum voltage on the bus. Conduction loss at high phase current, switching loss at the chosen frequency and cooling effort all count. The stage needs the voltage classes and large-current modules the vertical SiC MOSFET offers [3], [7]. The losses of IGBT and SiC inverters have been compared for 400 V and 800 V DC bus drivetrains [17]. One 300 kW, 800 V SiC inverter design reports a 2.85 % power-loss saving at 32 kW/L power density, with the baseline defined in that paper [5]. Short-circuit withstand and gate-oxide stability are the main reliability worries.

B. Onboard chargers

Chargers need compact magnetics, high power factor, and isolation, and weight and volume limits are strict [1]. Either technology can be employed with a bridgeless totem-pole power factor correction (PFC) stage and an isolated CLLC (capacitor-inductor-inductor-capacitor) or dual-active-bridge (DAB) stage. A 6 kW bidirectional charger using 600V GaN gate injection transistors has been published in a totem-pole PFC coupled to a variable-turns-ratio CLLC stage, and fits in 2 dm3 [6], a good illustration of what high frequency and low output charge can do. For 800V packs and higher power the isolated stage often requires 1200V devices, which favors SiC. Technology works either way, voltage class and frequency target decide.

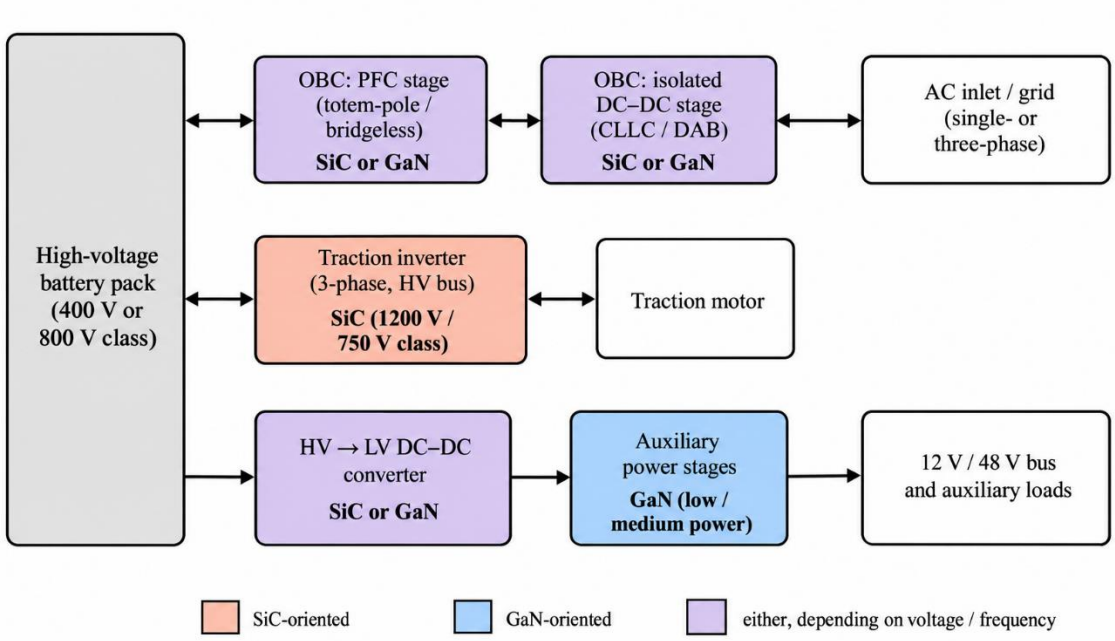

Fig. 4. Placement of SiC and GaN power devices in an EV powertrain. Colour shows the technology judged more suitable in the author's assessment (Table 3); the diagram is conceptual and does not imply a specific vehicle.

C. High-voltage DC–DC converters

The converter between the traction battery and the low voltage network balances switching frequency with passive component size and EMI. Higher frequency reduces transformer and filter size, but increases dv/dt and di/dt and increases common mode noise and layout sensitivity. The GaN data sheet specifies a dv/dt capability of 200 V/ns [4]. The filter and isolation barrier must be designed accordingly. SiC is employed when the high voltage side is 800V and the topology requires 1200V devices and GaN is used when the high voltage side can be built with 650V devices.

D. Auxiliary power converters

Auxiliary stages of low to medium power such as the 12 V or 48 V supply and the pump, fan and compressor drives gain from compactness and integration. Where lateral GaN devices are mature, voltages drop and the effort on gate drivers and layout can be spread over many units. SiC does not offer much in this regard so the real choice is between GaN and advanced silicon and cost generally decides it.

E. 800 V architectures

The pack voltage is increased to 800V, which reduces the current for a given power and so reduces cable and conduction loss, but adds to the insulation, creepage and transient-protection burden. The 1200V SiC device on an 800V bus has about 400V margin against switching overshoot and bus transients, and in the datasheet example of the 1200V device 8 mm of creepage is specified between drain and source in its package [7]. A 600V GaN device cannot simply replace it on 800V. Three-level or stacked topologies that halve the voltage per device could use it, but that is our own design inference and not a finding of the cited studies, and it adds switches and control complexity. The GaN example also lists surge and pulsed ratings above its continuous rating. They come with conditions and lifetime limits, so they should not be read as continuous capability [4].

Table 3: Application suitability of SiC and GaN power devices in EV subsystems (author's engineering assessment synthesized from [1], [4], [5], [6], [7], [17])

Subsystem	Typical bus class	Dominant design driver	SiC	GaN
Traction inverter	400–800 V; high current	Conduction loss, short-circuit withstand, cooling	Strong; 750–1200 V modules	Limited by voltage and current rating
OBC PFC stage	Mains-derived; ≈400 V link	Frequency, magnetics size, dead-time loss	Possible; 650–1200 V	Strong at 650 V; mature totem-pole examples [6]

Subsystem	Typical bus class	Dominant design driver	SiC	GaN
OBC isolated stage	Battery side 400–800 V	Soft switching, isolation, reverse conduction	Strong where 1200 V is needed	Strong at ≤ 650 V
HV DC–DC	400–800 V to 12/48 V	Frequency, EMI, passive size	Strong at 800 V	Possible; 650 V sides
Auxiliary	12–48 V; low/medium power	Compactness, integration, cost	Limited advantage	Strong
800 V architecture	800 V DC bus	Insulation, overshoot margin, topology	Direct fit with 1200 V	Needs multilevel or stacked topologies

6. COMPARATIVE DESIGN ANALYSIS AND ENGINEERING TRADE-OFFS

Table 2 and Table 3 put the comparison within the framework of devices and subsystems and four trade-offs keep recurring. SiC is rated 1200V and above at moderate switching speed. Lateral GaN switches faster at 650V and below. The gate drive is different: SiC requires a wide, asymmetric swing and tolerances of threshold drift while GaN requires a current-limited gate and a driver capable of controlling very fast edges [4], [7], [16]. Also the reverse conduction is different. The SiC body diode has a 4.6V drop at 25A but reverse-recovery charge. The GaN device has only output charge with conduction voltage of about 2.2V. Finally, the short switching times in GaN and large currents in SiC make loop inductance, layout and gate loop design critical [18].

Cost, manufacturing maturity and availability are also important factors. We do not quote figures for them because they depend on wafer size, yield, volume and supplier. It is easier to explain qualification. Stress-test qualification for discrete semiconductors in automotive applications is defined in the AEC-Q101 [19]. The GaN data sheet says other uses are the supplier's responsibility and references JEDEC-based industrial qualification [4]. Thus, a device described herein as a data point is not necessarily suitable for a vehicle. For a production design, a part with a qualification report is required to demonstrate compliance and a reliability analysis against the vehicle mission profile is required.

7. THERMAL MANAGEMENT, RELIABILITY, AND PACKAGING

Losses heat the junction, and temp changes resistance, energy switching and lifetime. Taking the coolant as the reference, a first-order steady-state estimate is

$$T_{\mathrm{j}} = T_{\mathrm{cool}} + P_{\mathrm{loss}}\left(R_{\theta \mathrm{JC}} + R_{\theta \mathrm{CC}}\right) \tag{12}$$

where T_{cool} is the coolant temperature, $R_{\theta JC}$ is the junction-to-case thermal resistance, and $R_{\theta CC}$ is the case-to-coolant thermal resistance including the interface material. Junction-to-ambient resistance suits only free-standing parts. The relation assumes steady state and uniform temperature, so it breaks down for short pulses. For those the transient thermal impedance

$$Z_{\theta \mathrm{JC}}(t) = \sum_{i=1}^{n} R_i\left(1 - \mathrm{e}^{-t/\tau_i}\right) \tag{13}$$

applies in Foster form as in (13), with R_i and τ_i fitted to the datasheet curve [4], [7]. For the SiC example at 100 kHz, 158.5 W of loss across $R_{\theta JC}$ = 0.32 °C/W lifts the junction about 51 °C above the case according to (12), so the case must stay below roughly 124 °C to respect the 175 °C limit. For the GaN example 7.5W across the maximum 1°C/W gives at most about 7.5°C. The real heat path through the package and board adds more resistance. Both calculations are based on the hypothetical operating points behind Fig. 3 and are not design limits.

The failure and degradation mechanisms that have been documented are different for the two technologies. Gate-bias stress induces a threshold voltage shift due to near-interfacial oxide traps in SiC MOSFETs [16]. Short-circuit events can destroy the device or degrade its parameters over repeated pulses. Short circuit failure mechanisms and test constraints are reviewed in [20]. For GaN HEMTs, trapping, gate degradation, and hot-electron effects are reviewed in [10], and dynamic on-resistance has been measured out to multi-megahertz frequencies on a sub-200 V device [15]. In both

cases the power-cycling and thermal-cycling lifetime is strongly dependent on the module materials and interconnects and not only on the die.

Parasitic loop inductance L_σ produces a turn-off overshoot

$$\Delta V \approx L_\sigma \frac{\mathrm{d}i}{\mathrm{d}t} \tag{14}$$

For the SiC example, a 50 A fall in 14 ns is about 3.6 A/ns, so (14) with an assumed 10 nH loop adds about 36 V on top of the bus voltage. The 10 nH value is an assumption chosen for illustration. Conventional wire-bonded modules hold back WBG performance through parasitic inductance and the heat-dissipation limits of aluminium wires, which has motivated low-inductance interconnects and better cooling paths [18]. At the board level, layout, Kelvin source connections, and careful gate loop design all address the same issue, and this issue becomes more significant as edge rates increase. With higher edge rates comes higher electromagnetic interference. Filter and layout design cannot be separated from the choice of device.

8. EMERGING TRENDS AND RESEARCH CHALLENGES

Presented here is evidence for five gaps.

Characterization of dynamic on-resistance. The sub-200V measured devices have been reported with multi-megahertz [15]. To reliably predict conduction loss in EV chargers, data under converter relevant conditions are required, including zero-voltage and hard switching, bus-voltage transients and long-term stress at 650V.

SiC gate reliability and short circuit protection Separate reports on threshold drift and short-circuit degradation exist [16], [20]. Their behavior under automotive gate-bias profiles and repeated protected short circuits, as well as the design of fast detection circuits compatible with the short withstand time of the devices, remains an open question.

Integration and low inductance package. The packaging reviews state that low parasitic inductance and efficient cooling are open challenges for SiC modules [18]. The same issues hold for GaN co-packaged with its driver. There is a clear gap in the evaluation of embedded and planar approaches in automotive power cycling.

Advanced gate drivers, sensing and condition monitoring. [5] describes the design of a 300 kW, 800 V SiC inverter with adjustable gate-drive strength, protection and state-of-health monitoring of modules. The question of which measurable quantity, eg the threshold voltage or the on-resistance, is the best indicator of aging in service, and how a driver should respond to it, is not resolved.

AI-Based Optimization and Multiphysics Electrothermal Modeling. We could optimize the whole converter using models of coupling device, circuit, magnetics and cooling, rather than optimizing each component separately. Machine-learning surrogates for such models are promising but no evidence is provided in the present paper for their performance in this field.

9. CONCLUSIONS

Comparing vertical SiC MOSFETs with lateral GaN HEMTs shows that the better choice depends on the application, not on the material. SiC suits high-voltage, high-current stages such as traction inverters and 800 V architectures, where 1200 V-class ratings and large-current modules are needed. Its main concerns there are gate-oxide stability and short-circuit withstand. GaN can pay off in compact, high-frequency stages at 650 V and below, such as onboard-charger PFC and isolated stages and auxiliary converters, where low gate charge and output charge cut switching loss. Its main concerns are dynamic on-resistance, gate-drive design, and layout. In the datasheet examples analysed here, switching loss overtakes conduction loss above roughly 43 kHz for the SiC device and 74 kHz for the GaN device under the stated conditions, and the GaN figure is an estimate.

The analysis supports five recommendations.

1) Filter devices by voltage class, current, frequency and topology. Match ratings and stated test conditions for candidate comparison.

2) Evaluate efficiency and power density at the converter level including magnetics, capacitors, cooling and filters, before giving a gain credit to the semiconductor.

3) Treat reverse-conduction loss, gate-drive range, and loop inductance as primary design inputs, not as details to fix at layout.
4) Ask for explicit automotive qualification evidence and a mission-profile reliability analysis for every production part.
5) Use GaN data that match the voltage class and frequency of the application, because dynamic on-resistance measured on low-voltage devices does not transfer directly to 650 V.

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